Design of a P4VT-Optimal Nano-CMOS Voltage Controlled Oscillator

Saraju P. Mohanty
Computer Science and Engineering
University of North Texas, Denton, TX 76203, USA.
Email: saraju.mohanty@unt.edu
Elias Kougianos
Electrical Engineering Technology
University of North Texas, Denton, TX 76203, USA.
Email: eliask@unt.edu
Garima Thakral
Computer Science and Engineering
University of North Texas, Denton, TX 76203, USA.
Email: gt0024@unt.edu
Priyadarsan Patra
Validation Research Lab
Intel Corporation, Hillsboro, OR 97124, USA.
Email: priyadarsan.patra@intel.com

Abstract

Because of temperature effects, existing Radio-Frequency Integrated Circuit (RFIC) design methodologies are deviating further away from the reality of how today's silicon behaves. Constant on-chip temperature can no longer be assumed. Analysis of temperature effects indicates where a design must be optimized. We present the design flow for a Power-Performance-Process-Parasitic-Voltage-Temperature (P4VT) aware Voltage Controlled Oscillator (VCO) for dual-V_{Th} nano-CMOS technologies. Through simulations, we have shown that parasitics, process, voltage and temperature have a drastic effect on the performance (center frequency) of the VCO. A design optimization of the VCO, along with dual-threshold power minimization has been performed in the presence of worst case process-voltage-temperature conditions. The end product of the proposed methodology is a P4VT aware performance optimized dual threshold $90nm$ VCO physical design. We have achieved 16.4% power (including leakage) minimization with 10% degradation in center frequency compared to the target frequency, in presence of *worst-case* P4VT and parasitics. To the best of the authors' knowledge, this is the first research reporting a dual-threshold nanoscale CMOS VCO design optimized for power (including leakage), performance, parasitics, process, voltage and temperature.

Index Terms

Voltage Controlled Oscillator, Nanoscale CMOS, Process Variation, Power Aware Design, Performance Aware Design, Parasitic Aware Design, Dual-Threshold Voltage

I. Introduction, Motivation, and Contributions

A dichotomy exists in the design of Radio Frequency Integrated Circuits (RFICs): they must be simultaneously low power and high performance. Minimum power expenditure is expected concurrently with performance today. The goal of power-aware design is to minimize power consumption while meeting performance requirements. Therefore, as power dissipation increases, the cost of power delivery to the ever-increasing number of transistors on a chip multiplies rapidly.

The impact of process variation on performance factors of a design is much more severe for nanometer technologies [1]. Just as in digital design where interconnect delays make or break a design, the move to $90nm$ and lower process technologies means that the variations in process parameters have a significant effect on the performance metrics of analog/mixed-signal, memory and RF circuits.

In addition, the numerous parasitic effects induced by layout, especially for high performance and high speed circuits, pose a problem for RFIC design. Lack of exact layout information during circuit sizing leads to long design iterations involving time consuming runs of complex tools. The traditional IC

design flow involves repetitive iterations of circuit sizing, layout generation, parasitic value extraction, and performance evaluation. Redesign is needed whenever the final performance does not conform to the specification. In order to improve design efficiency and reduce the time-to-market, it is crucial to be able to predict parasitic effects for accurate performance.

Another emerging critical issue due to technology scaling is the effect of on-die temperature variation. What was previously a second-order effect that could be adequately addressed with a few corner cases and guard-bands has now become a first-order effect. It interacts with a number of these other issues in ways that make analysis difficult. There is a need for new, temperature-aware design methodologies in order to produce properly functioning and reliable first silicon. Both power dissipation and operating frequency are worsened at high temperatures due to the increase of leakage currents and the reduction of carrier mobility. The challenge for RF design is the centering of a design including PVT variations [2]. By integrating temperature-aware capabilities into today's design flows, there is no need to reinvent analysis standards that have been established during the past decades. Instead, through the use of tools that incrementally retrofit today's flows with temperature aware data, the temperature effects can be fully accounted for. Applying thermal analysis reduces pessimism or risk associated with the assumption of a uniform on-chip temperature. A temperature-aware design flow is useful for existing technologies down to $90nm$, and is required for technologies below $90nm$.

In this paper we address these issues by proposing a new P4VT (power-performance-process-parasitic-voltage-temperature) optimization methodology for RFIC circuits, using a CMOS Voltage Controlled Oscillator as a case study. This paper focuses on center frequency optimization of VCO, as it is a critical performance parameter. The **novel contributions of this paper** are as follows:

1) We propose a Power-Performance-Parasitic-Process-Voltage-Temperature (P4VT) aware optimization flow for nanoscale CMOS analog circuits.
2) The design of a P4VT aware RF nano-CMOS VCO is presented.
3) For power optimization of the VCO, we apply a judicious dual-threshold level process technique. The dual-threshold technique is an effective means for minimizing the power of a circuit [3], where high-threshold transistors consume less power than low-threshold transistors.
4) A dual-threshold physical design of the VCO is presented.

The rest of the paper is organized as follows. Related research works are discussed in section II. Section III presents the P4VT aware optimization flow of VCO. The proposed P4VT flow is discussed in section III. Section IV discusses the baseline logical design of the VCO. Process variation analysis

is discussed in section V. P4VT optimization is presented in section VI. The paper is concluded with directions for future research in section VII.

II. Related Prior Research

A tabular comparison of our research with existing literature (Table I) reveals our design to be a low power, high-performance VCO at nanoscale technology.

TABLE I

VCO PERFORMANCE COMPARISON

Reference	Technology	Performance	Power
Troedsson [4]	$250nm$	$2.4GHz$	$5.5mW$
Tiebout [5]	$250nm$	$1.8GHz$	$20mW$
Dehghani [6]	$250nm$	$2.5GHz$	$2.6mW$
Long [7]	$180nm$	$2.4GHz$	$1.8mW$
Kwok [8]	$180nm$	$1.4GHz$	$1.46mW$
Ghai [9]	$90nm$ dual-T_{ox}	$2.3GHz$	$158\mu W$
Ghai [10]	$90nm$	$2.54GHz$	$--$
This Paper	$90nm$ dual-V_{Th}	$2.4GHz$	$137.5\mu W$

In [11], novel circuit level techniques using adaptive supply voltage and a body-bias voltage generating technique is proposed to achieve PVT variation tolerant designs. In [12], an operational amplifier used in a switch capacitor integrator is designed to be insensitive to PVT variations using corner analysis. A new all-digital-PLL for fast frequency acquisition is proposed in [13], where the digital controlled oscillator codeword is predicted by measuring the PVT variations. A PVT tolerant digital PLL is presented in [14], that has output frequency ranging from $0.18MHz$ to $600MHz$. An LC-VCO is presented in [15] that uses an automatic amplitude control circuit to minimize influence of PVT variations. A PVT tolerant PLL architecture which uses two on-chip digital calibration circuits to maintain loop transfer function is presented in [16].

There is a significant amount of research in the area of parasitic aware synthesis to overcome device and package parasitic degradations and to achieve optimal performance [17], [18]. This is due to high sensitivity of RFIC design to layout parasitics. Simulated annealing based approach is proposed in [19]

for synthesizing RF power amplifiers. Particle swarm optimization techniques are proposed for parasitic aware design in [20]. In [21], an LC VCO has been subjected to a parasitic-aware synthesis. A parasitic and process aware design flow has been proposed in [10]. In [22], the center frequency of a VCO has been optimized using a Design of Experiments (DOE) approach. The simulation-based circuit synthesis example in [23] does not include the layout parasitics in the design.

Accounting Process variation in analog circuits [24] and their power aware design are on the research forefront now. In [25], an analysis of the process parameters affecting a ring oscillator's frequency performance is presented. In [1], a current-controlled oscillator has been subjected to process variations. In [26], a dual-oxide technique for power and delay optimization is proposed at circuit level but do not address temperature effects. In [3], the effects of simultaneous variation of supply and process parameters are discussed on power consumption of datapath components.

This archival journal paper is based on the shorter blind peer-reviewed conference paper [27]. The current journal paper provides substantially expanded details on the design methodology for the VCO. The modified conjugate gradient optimization algorithm used to obtain the final design is further elaborated. The overall design of the VCO is presented in detail.

III. P4VT Aware Design Flow

The P4VT design flow (figure 1) accounts for parasitic, process, power, performance, voltage and temperature in the VCO circuit.

First, the logical design is done to meet the required center frequency (target f_0) specification of $f_0 \geq$ 2GHz. Using the device dimensions from the logical design, a preliminary physical design is prepared and is subjected to Design Rule Check (DRC), LVS (Layout versus Schematic) and parasitic (RCLK) extraction. A worst case process, voltage, and temperature analysis of the parasitic extracted preliminary physical design with respect to performance (center frequency) is carried out, where the worst case process is identified and the physical design is subjected to it. Figure 2(a) shows the behavior of VCO center frequency (f_0) with respect to temperature (measured at 27°C, 50°C, 75°C, 100°C and 125°C). The VCO is subjected to process-voltage variation at each of these temperatures (using Monte-Carlo simulations). Hence, we can observe the behavior of the $\mu(f_0)$, $\mu(f_0) + 3 \times \sigma$ and $\mu(f_0) - 3 \times \sigma$ with temperature (μ = mean, σ = standard deviation). It is clear from figure 2(a), that the center frequency moves away from the target f_0; it reduces with increase in temperature.

This is followed by high-threshold voltage assignment (HV_{Thn},HV_{Thp}) to the power-hungry transistors (NMOS, PMOS) of the VCO using the *High threshold model file*. The rest of the transistors in the circuit

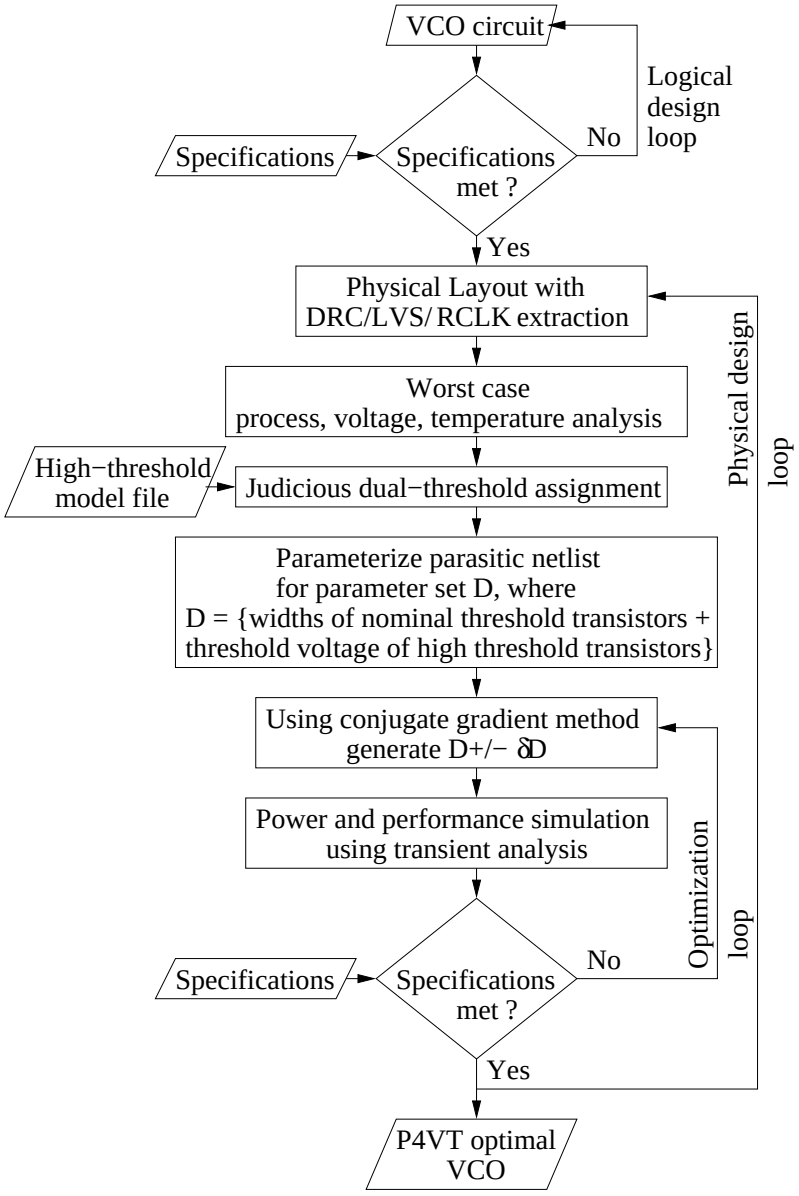


Fig. 1. The Proposed RFIC P4VT Optimal Design Flow

operate on the *baseline model file*. We call this technique "judicious dual-threshold assignment", used to minimize the power consumption of the VCO circuit [3]. The netlist obtained from the preliminary physical design is then parameterized for parameter set D (widths of transistors and HV_{Thn}, HV_{Thp}). We call this "parameterized parasitic netlist". The parameterized parasitic netlist is then subjected to a modified conjugate gradient based optimization loop in order to meet the specifications (performance, power) in a worst case P4VT environment. The details of the optimization algorithm are given in

algorithm 1. Once the parameter values for which the specifications are met are obtained, a final physical design of the VCO is created using these parameter values. Hence we obtain a P4VT optimal dual-threshold VCO layout from the proposed design flow. From figure 2(b), we can observe that f_0 meets the target specifications of f_0 $\geq$2GHz (with a 10% degradation at worst case) *across the entire specified temperature range*.

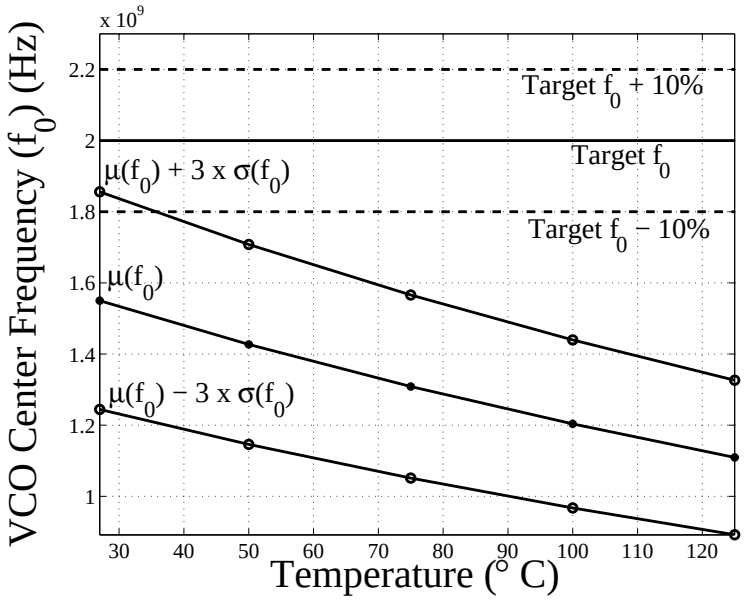
Algorithm 1 Modified conjugate gradient algorithm

1: **Input:** Arbitrary parameter set starting $\mathbf{x}^{(0)}$, maximum number of iterations n, objective function $q(\mathbf{x}) = c + \mathbf{b}^T + \frac{1}{2}\mathbf{x}^T\mathbf{B}\mathbf{x}$, gradient function $\mathbf{g} = \mathbf{b} + \mathbf{B}\mathbf{x}$ of objective function.
2: **Output:** Optimized parameter set $\mathbf{x}$.
3: $k = 0$.
4: Start in steepest descent direction $\mathbf{s}^{(0)} = -\mathbf{g}^{(0)}$, where $\mathbf{g}^{(0)} = \mathbf{g}(\mathbf{x}^{(0)})$.
5: **while** $(k < n)$ **do**
6: Calculate scalar factor t_k^* to move along direction of steepest descent: $t_k^* = -\frac{\mathbf{s}^{(k)T}\mathbf{g}^{(k)}}{\mathbf{s}^{(k)T}\mathbf{B}\mathbf{s}^{(k)}}$.
7: Find the minimum point along direction $\mathbf{s}^{(k)}$: $\mathbf{x}^{(k+1)} = \mathbf{x}^{(k)} + t_k^*\mathbf{s}^{(k)}$.
8: Calculate gradient at the turning point: $\mathbf{g}^{(k+1)} = \mathbf{g}(\mathbf{x}^{(k+1)})$.
9: Compute modified norm ratio: $h_k = \frac{[\mathbf{g}^{(k+1)}]^T[\mathbf{g}^{(k+1)} - \mathbf{g}^{(k)}]}{[\mathbf{s}^{(k)}]^T[\mathbf{g}^{(k+1)} - \mathbf{g}^{(k)}]}$.
10: Find new direction: $\mathbf{s}^{(k+1)} = -\mathbf{g}^{(k+1)} + h_k\mathbf{s}^{(k)}$.
11: **end while**
12: Record $\mathbf{x}^{(k+1)}$.

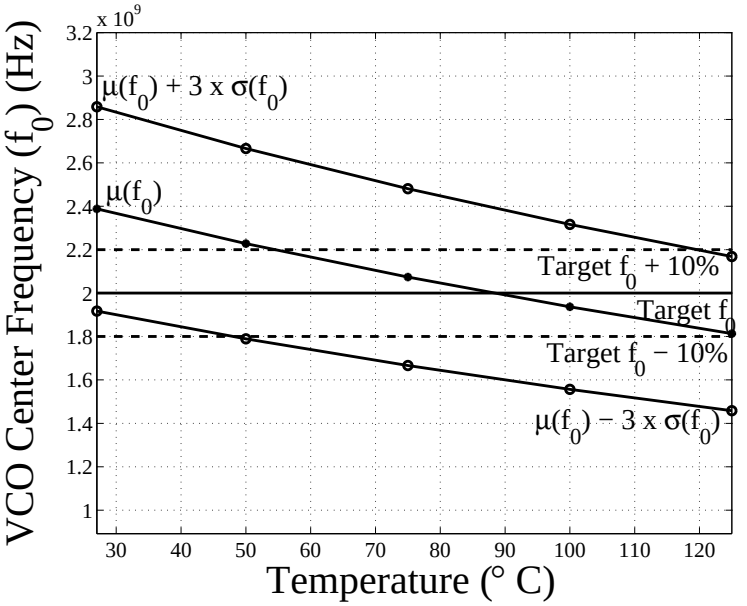
IV. Transistor Level Design of the VCO

We have considered a current starved VCO in this work. The VCO design (figure 3(a)) comprises of three stages: (1) input stage consisting of two transistors with high impedance, (2) an odd numbered chain of inverters along with two current source transistors per inverter, which limit the current flow to the inverter and (3) buffer stage. The circuit has no stable operating point and it will oscillate at some frequency that is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter, which is dependent upon the input voltage to the VCO. The operating frequency of the VCO, f_0 can be determined using the relation [28]:

$$f_0 = \left(\frac{1}{N \times T_t}\right) = \left(\frac{I_{inv}}{N \times C_t \times V_{DD}}\right), \tag{1}$$



(a) For non-optimized VCO



(b) For P4VT optimized VCO

Fig. 2. VCO Center Frequency (f_0) versus Temperature Chart.

where V_{DD} is the supply voltage, I_{inv} is the current flowing through the inverter, N is the odd number of inverters in the VCO circuit, T_t is the total time required to charge or discharge the capacitance of each stage of an inverter and C_t is the total capacitance given by the sum of the input and output capacitances of the inverter. T_t is the sum of two times: t_1, which is the time to charge C_t from 0 to the inverter switching point, V_{sw} , and t_2, which is the time to discharge C_t from V_{DD} to V_{sw}. Assuming that the same current, I_{inv}, flows through the PMOS and NMOS during the charging and discharging, respectively, the two times can be calculated as:

$$t_1 = C_t \times \left(\frac{V_{sw}}{I_{inv}}\right), \tag{2}$$

$$t_2 = C_t \times \left(\frac{V_{DD} - V_{sw}}{I_{inv}}\right). \tag{3}$$

Since T_t = t_1 + t_2, combining equations 2, 3 and inserting the expresion of T_t in equation 1, we get the required expression.

The operating frequency of the VCO can be mainly controlled by an applied DC input voltage, which adjusts the current I_{inv} through each inverter stage. The expression for C_t is:

$$C_t = \left(\frac{5}{2}\right) \times C_{ox} \times (W_p \times L_p + W_n \times L_n), \tag{4}$$

where C_{ox} is the gate oxide capacitance per unit area, W_n and W_p are the widths and L_n and L_p are the lengths of the inverter NMOS and PMOS transistors, respectively. C_{ox} is formulated as:

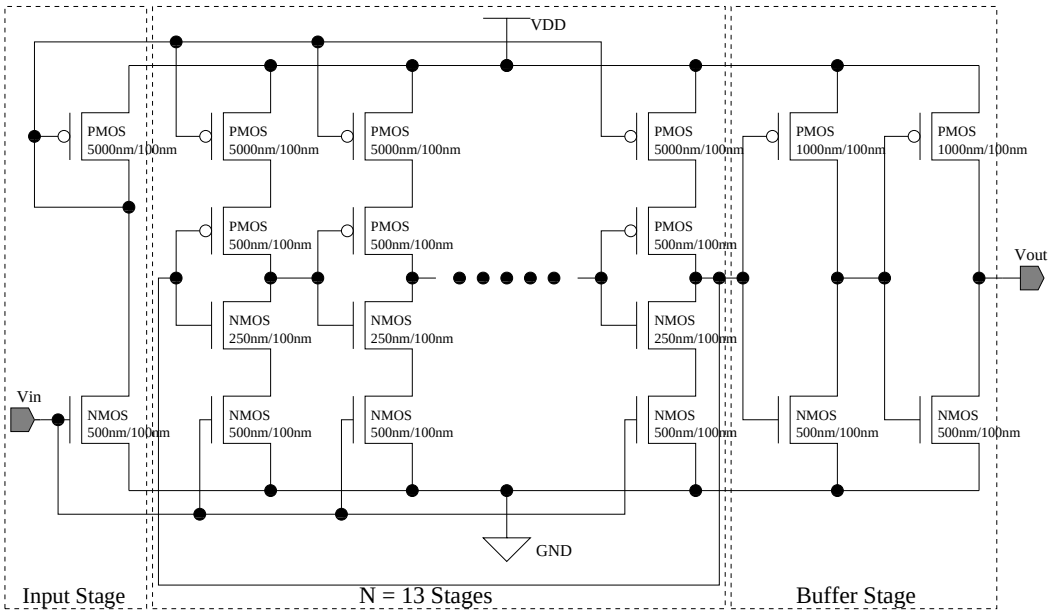
$$C_{ox} = \left(\frac{\epsilon_{SiO_2} \times \epsilon_0}{T_{ox}}\right), \tag{5}$$

where ϵ_{SiO_2} is the relative dielectric constant of SiO_2, ϵ_0 is vacuum dielectric constant and T_{ox} is the gate oxide thickness.

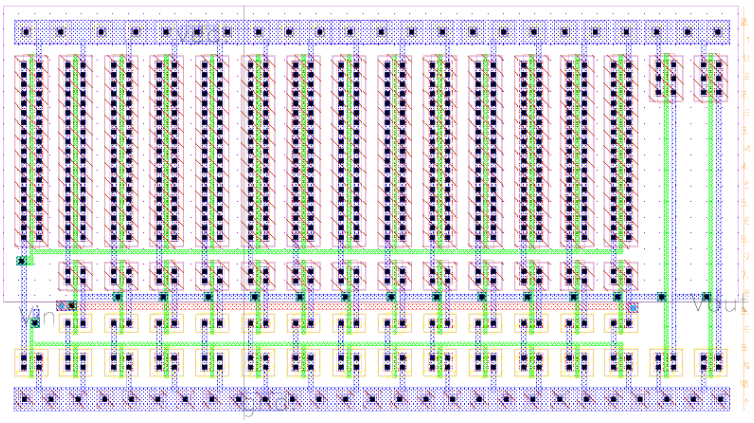
The functional specification for this design is the center frequency. The target center frequency has been kept at a minimum of 2 GHz. The number of stages is fixed to 13 for high frequency requirement. For baseline design, we have chosen L_n = L_p = 100 nm, W_n = 250 nm and W_p = 2 $\times$ W_n = 500 nm. C_t is calculated using equation 5. Finally, I_{inv} is calculated using equation 1, and the current starved NMOS and PMOS devices are sized to provide the required current I_{inv}. Thus we obtained L_{ncs} = L_{pcs} = 100 nm, and W_{ncs} = 500 nm and W_{pcs} = 10 $\times$ W_{ncs} = 5μm, where W_{ncs} and W_{pcs} are the widths and L_{ncs} and L_{pcs} are the lengths of the current-starved NMOS and PMOS transistors, respectively.

From these equations, we obtain the minimum sizes of transistors needed for successful operation.

The preliminary physical design of the VCO is then carried out using these transistor sizes. It occupies an area of 228.43μm^2, shown in figure 3(b).



(a) Logical design



(b) Physical design

Fig. 3. Baseline Design of the VCO for $90nm$.

V. Process-Voltage Variation Analysis of VCO

For process-voltage variation, we have considered variation in 5 parameters, namely: (1.)V_{DD}: Supply voltage, (2.) V_{Thn}: NMOS threshold voltage, (3.) V_{Thp}: PMOS threshold voltage, (4.) T_{oxn}: NMOS gate oxide thickness, (5.) T_{oxp}: PMOS gate oxide thickness. A correlation coefficient (cc) of 0.9 is assumed between T_{oxn} and T_{oxp}. Each of these process parameters is assumed to have a Gaussian distribution with mean (μ) taken as nominal value specified in the process design kit, and a standard deviation (σ) of 10% of the mean is assumed. The VCO is subjected to Monte Carlo (MC) simulations for N = 1000 runs at temperature T, where T = 27°C, 50°C, 75°C, 100°C and 125°C. The methodology is shown in figure 4.

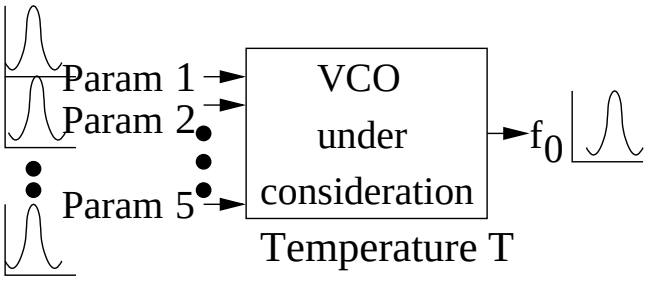


Fig. 4. Methodology for process-voltage variation at given temperature T.

The mean ($\mu(f_0)$) and standard deviation ($\sigma(f_0)$) for f_0 are recorded at each temperature. At 27°C (room temperature), the center frequency (f_0) is observed to have a Gaussian distribution with μ = 1.54GHz and σ = 103.5MHz. The plot is shown in figure 5.

The worst case process for f_0 is identified to be the one where process parameters (V_{Thn}, V_{Thp}, T_{oxn}, T_{oxp}) are increased by 10%. The worst case voltage is where V_{DD} is reduced by 10%. The worst case temperature is 125°C.

VI. P4VT Optimization of the VCO

In this section, we demonstrate how the performance (f_0) discrepancy is overcome along with power minimization of the VCO using a dual-oxide technique. After full-extraction($RCLK$), a 22% degradation in the performance (center frequency) is observed between the preliminary physical design and target frequency. Furthermore, a 50% discrepancy is observed between the preliminary physical design and target frequency when the VCO is subjected to *worst case process-voltage-temperature* (wcP4VT) (section V). Details are given in Table II.

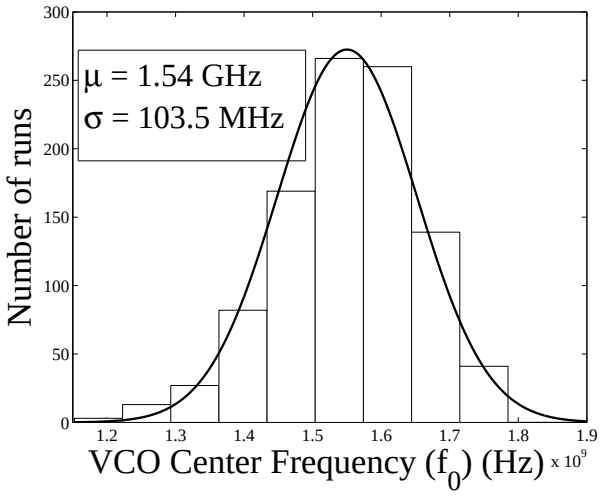


Fig. 5. Statistical Distribution of f_0 for process-voltage variation at room temperature (27°C).

TABLE II

RESULTS SHOWING PERFORMANCE DISCREPANCY AND WORST CASE PROCESS VALUES FOR A TARGET FREQUENCY $\geq 2GHz$

Parameter	Preliminary Physical Design	Preliminary Physical Design + wcP4VT	Final Physical Design + wcP4VT
f_0	1.56GHz	1GHz	1.8GHz
discrepancy	22%	50%	10%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
V_{Thn}	$0.169V$ (nominal)	$0.186V$ $(+10\%)$	$0.186V$
V_{Thp}	$-0.136V$ (nominal)	$-0.145V$ $(+10\%)$	$-0.145V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ $(+10\%)$	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ $(+10\%)$	$2.728nm$

Hence we obtain:

- Target center frequency $f_0 \geq 2GHz$.
- Preliminary Physical design center frequency $f_{0\mathrm{p}} = 1.56GHz$.
- Preliminary Physical design center frequency in worst case P4VT conditions $f_{o\mathrm{P4VT}} = 1GHz$.
- Initial average power consumption (including leakage) $P_{VCO} = 164.5\mu W$.

A. Judicious dual-threshold assignment

A transient analysis is performed on the physical design of the VCO, and the average power consumed by all transistors is measured. The input stage transistors (shown by solid circles in figure 6) collectively consume 48% of the total average power of the VCO circuit, hence are most suitable candidates for higher threshold voltage assignment (HV_{Thn}, HV_{Thp}). The buffer stage transistors (shown by dashed circles in figure 6) consume 11.5% of the total average power, and hence may be treated to higher threshold voltage, for further power minimization. In this paper, we have subjected the input stage transistors to dual-threshold assignment. These transistors follow a different model file called *High threshold model file*. The other transistors in the VCO circuit follow the *Baseline model file*.

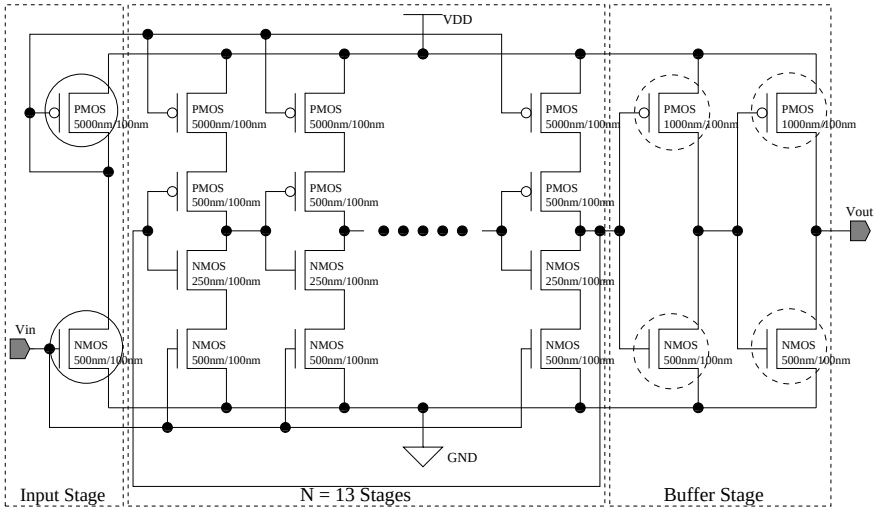


Fig. 6. Possible candidate transistors for judicious dual-threshold assignment.

B. Parameterizing the Parasitic Netlist

Followed by the dual-threshold assignment, the parasitic-aware netlist generated from the preliminary layout is then parameterized with respect to the optimization parameters. The parameter set includes the

widths of PMOS and NMOS devices in the inverter (W_n, W_p), the PMOS and NMOS devices in the current-starved circuitry (W_{ncs}, W_{pcs}), and HV_{Thn}, HV_{Thp}.

C. Power-performance Optimization

After parametrization of the netlist, it is subjected to power-performance optimization using a conjugate gradient method, where the parameter set takes on different values, till the specifications are met. The conjugate gradient method has been used as it has low memory requirements and high convergence speed [29]. The candidates for optimization are the widths of the inverters (W_n, W_p) and current-starved transistors (W_{ncs}, W_{pcs}), and the threshold voltages (HV_{Thn}, HV_{Thp}) of high-threshold (input stage) transistors. While the higher threshold voltages minimize power consumption of VCO, the higher widths of the devices maximize performance. Our objective set is $f_0 \geq$ 2GHz, and $P_{VCO} = minimum$. The algorithm is shown in algorithm 2. Table III shows the final values of the parameter set for P4VT optimal VCO. S is the stopping criteria for the optimization to stop when the objective set is within $\pm\epsilon$ (where ϵ is designer specified error margin, in percentage). For our design, we have taken $\epsilon = 10\%$. The outputs of the algorithm are the optimized objective set F_{opt} which satisfies the stopping criteria S, and the optimal values of the design variable set D_{opt} within the upper and lower design constraints.

The algorithm starts out with a guess of D, and then it performs iterations, improving the guess at each one, until the guess is close enough and the objective set F_{opt} is met with the stopping criteria S.

TABLE III

TABLE SHOWING OPTIMIZED VALUES OF THE PARAMETER SET

D	C_{low}	C_{up}	D_{opt}
W_n	$200nm$	$500nm$	$390nm$
W_p	$400nm$	$1\mu m$	$445nm$
W_{ncs}	$1\mu m$	$5\mu m$	$10\mu m$
W_{pcs}	$5\mu m$	$10\mu m$	$30\mu m$
HV_{Thn}	$0.1692662V$	$0.5V$	$0.5V$
HV_{Thp}	$-0.5V$	$-0.1359511V$	$-0.4975V$

The final physical design of the VCO is then carried out using these parameter values, and the following results are obtained:

- Target center frequency $f_0 \geq 2GHz$.

Algorithm 2 Power-Performance optimization algorithm for VCO

Input: Parasitic Aware netlist, Baseline model file, High threshold model file, Worst case P4VT settings, Objective set $F = [f_0, P_{VCO}]$, Stopping criteria S, parameter set $D = [W_n, W_p, W_{ncs}, W_{pcs}, HV_{Thn}, HV_{Thp}]$, Lower parameter constraint C_{low}, Upper parameter constraint C_{up}.
Output: Optimized objective set F_{opt}, Optimal parameter set D_{opt} for stopping criteria $S \leq \epsilon$. {where $\epsilon = 10\%$}
Perform first iteration with initial guess of D.
while ($C_{low} < D < C_{up}$) **do**
    Use conjugate gradient to generate D' = $D \pm \Delta D$ in the direction of travel of $F_{opt} \pm \epsilon$.
    Compute $F(D')$ = [f_0, P_{VCO}].
    Compute S as the difference of target objective set and current objective set.
    if $S \leq \epsilon$ **then**
        {stopping criteria is within the error margin}
        return D_{opt} = D'.
    end if
end while
Using D_{opt}, construct final physical design and simulate.
Record F_{opt}.

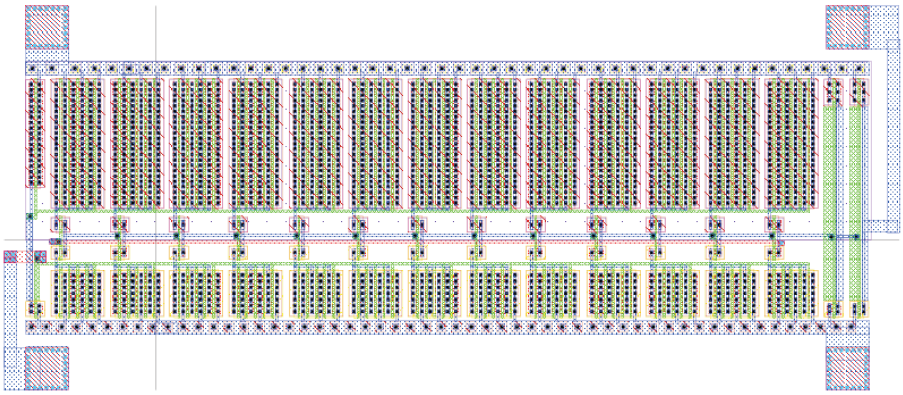
- Final Physical design center frequency $f_{0\mathrm{p}} = 2.4GHz$.
- Final Physical design center frequency in a worst case P4VT conditions $f_{0\mathrm{P4VT}} = 1.8GHz$.
- Final average power consumption (including leakage) $P_{VCO} = 137.5\mu W$

Hence we obtained a final optimized dual-threshold layout, with $1.8GHz$ center frequency under worst case P4VT conditions, and $2.4GHz$ center frequency in nominal P4VT conditions and 16.4% power minimization. The conjugate gradient optimization converged in 8 iterations, with each iteration typically lasting 4 minutes.

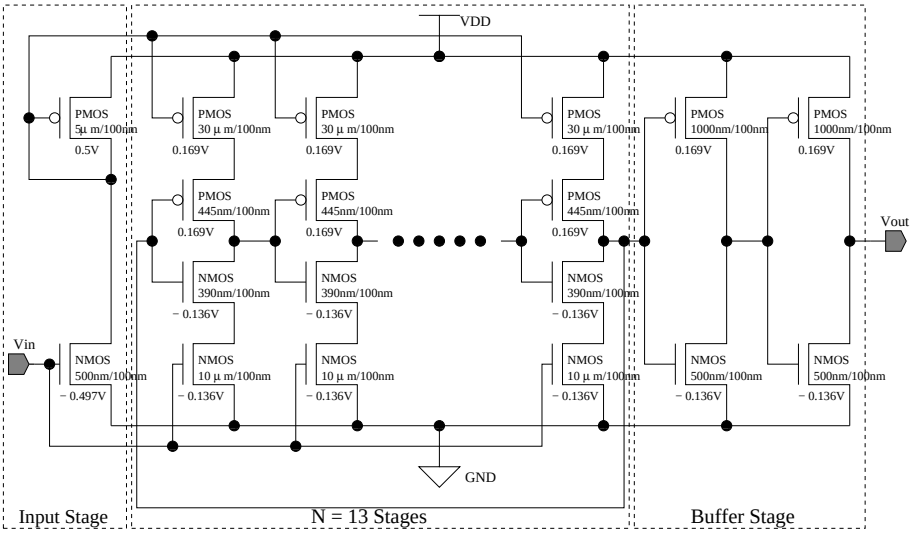
D. P4VT optimal dual-threshold layout of the VCO

The dual-threshold physical design of the VCO has been performed using a generic 90 nm Salicide 1.2V/2.5V 1 Poly 9 Metal process design kit. At high frequencies, parasitic inductance has a major

impact on chip performance. Hence it is necessary to extract self (L) and mutual (K) inductance so that the impact of inductive coupling could be assessed and minimized on the layout. A full extraction of the layout was carried out (including resistors (R), capacitors (C), inductors (L) and mutual inductors (K)). The P4VT optimal physical design is shown in figure 7(a). It occupies an area of $547.74\mu m^2$. There is an area penalty of 58.3% over the preliminary physical design. The final optimal widths of the P4VT optimal circuit and high threshold transistors are shown in figure 7(b).



(a) P4VT optimal dual-threshold layout of the VCO.



(b) Optimal widths and threshold voltages of transistors of the P4VT optimal VCO.

Fig. 7. P4VT optimal dual-threshold design of the VCO.

The performance summary of the VCO is given in Table IV.

TABLE IV

MEASURED PERFORMANCE OF THE VCO

Parameter	Value
Technology	$90nm$ CMOS $1P$ $9M$
Supply Voltage (V_{DD})	$1.2V$
center frequency (Nominal P4VT)	$2.4GHz$
Worst case P4VT	V_{Th} ($+10\%$), T_{ox} ($+10\%$), V_{DD} (-10%), 125°C
center frequency (worst case P4VT)	1.8GHz
Parameter set	6 (W_n, W_p, W_{ncs}, W_{pcs}, HV_{Thn}, HV_{Thp})
Number of objectives	2 ($f_0 \geq$ 2GHz, P_{VCO}=$minimum$)
Area occupied	547.74μm^2 (58.3% penalty)

VII. CONCLUSIONS AND FUTURE RESEARCH

We presented the design flow for a P4VT (Power-Performance-Parasitic-Process-Voltage-Temperature) optimal nano-CMOS VCO. Our proposed design flow can be implemented on top of existing electrical analysis and physical design tools. This provides for the analysis of temperature effects at an early stage in the design cycle. The center frequency has been treated as the target specification. The degradation of the center frequency due to worst case P4VT effects has been narrowed down from 50% to 10%, along with 16.4% power minimization using a dual-threshold technique. The end product of the proposed design flow is a P4VT optimal dual-threshold VCO physical design that meets the functional specifications across the entire range of expected temperatures. As part of extension of this research, we plan to propose a P5VT optimal methodology, where the 5th P would be phase noise.

ACKNOWLEDGMENTS

This research is supported in part by NSF award number CNS-0854182 and SRC award number P10883. The authors would like to acknowledge Dhruva Ghai for his inputs.

REFERENCES

[1] KIM D., CHOONGYEUN C., JONGHAE K., PLOUCHART J.-O., TRZCINSKI R., AHLGREN D.: 'CMOS Mixed-Signal Circuit Process Variation Sensitivity Characterization for Yield Improvement'. In: Proceedings of the IEEE Custom Integrated Circuits Conference; 2006. p. 365–368.

[2] CHOI K., ALLSTOT D.J.: 'Post-optimization design centering for RF integrated circuits'. In: Proceedings of the International Symposium on Circuits and Systems; 2004. p. 956–959.

[3] MOHANTY S.P., KOUGIANOS E., GHAI D., PATRA P.: 'Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano- CMOS circuits under Process Variation'. In: Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis; 2007. p. 207–213.

[4] TROEDSSON N., SJOLAND H.: 'High performance 1 V 2.4 GHz CMOS VCO'. In: Proceeedings of the IEEE Asia-Pacific Conference on ASIC; 2002. p. 185–188.

[5] TIEBOUT M.: 'Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS'. *IEEE Journal of Solid-State Circuits*. 2001 July; **36**(7):1018–1024.

[6] DEHGHANI R., ATARODI S.M.: 'Optimised analytic designed 2.5GHz CMOS VCO'. *IEE Electronic Letters*. 2003 August; **39**(16):1160–1162.

[7] LONG J., FOO J.Y., WEBER R.J.: 'A 2.4 GHz Low-Power Low-Phase-Noise CMOS LC VCO'. In: Proceedings of the IEEE Computer Society Annual Symposium on VLSI; 2004. p. 213.

[8] KWOK K., LUONG C.H.: 'Ultra-low-Voltage high-performance CMOS VCOs using transformer feedback'. *IEEE Journal of Solid State Circuits*. 2005 March; **40**(3):652–660.

[9] GHAI D., MOHANTY S.P., KOUGIANOS E.: 'Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO'. In: Proceedings of the Great Lakes Symposium on VLSI; 2009. p. 303–308.

[10] GHAI D., MOHANTY S.P., KOUGIANOS E.: 'Design of Parasitic and Process-Variation Aware Nano-CMOS RF Circuits: A VCO Case Study'. *IEEE Transactions on Very Large Scale Integration Systems*. 2009 September; **17**(9):1339–1342.

[11] KIM K.K., KIM Y.B.: 'A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems'. *IEEE Transactions on Very Large Scale Integration Systems*. 2009 April; **17**(4):517–528.

[12] CHARAN K., PANDA A.K., NOOR A., SABHARWAL S.: 'Design of a Humidity sensor with PVT Variations using AMI C5 CMOS Technology'. In: Proceedings of the International Conference on Recent Advances in Microwave Theory and Applications; 2008. p. 839–842.

[13] JEON H.S., YOU D.H., PARK I.C.: 'Fast frequency acquisition all-digital PLL using PVT calibration'. In: Proceedings of the International Symposium on Circuits and Systems; 2008. p. 2625–2628.

[14] LIN J., HAROUN B., FOO T., WANG J.-S., HELMICK B., RANDALL S., MAYHUGH T., BARR C., KIRKPATRIC, J.: 'A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process'. In: Proceedings of the International Solid State Circuits Conference; 2004. p. 488–541.

[15] MIYASHITA D., ISHIKURO H., KOUSAI S., KOBAYASHI H., MAJIMA H., AGAWA K., HAMADA M.: 'A Phase Noise Minimization of CMOS VCOs over Wide Tuning Range and Large PVT Variations'. In: Proceedings of the International Custom Integrated Circuits Conference; 2005. p. 583–586.

[16] KONDOU M., MORI T.: 'A PVT Tolerant PLL with On-Chip Loop-Transfer-Function Calibration Circuit'. In: Proceedings of the International Symposium on VLSI Circuits; 2007. p. 232–233.

[17] PARK J., CHOI K., ALLSTOT D.J.: 'Parasitic-aware design and optimization of a fully integrated CMOS wideband amplifier'. In: Proceedings of the Asia South Pacific Design Automation Conference; 2003. p. 904–907.

[18] BALLWEBER B.M., GUPTA R., ALLSTOT D.J.: 'A fully integrated $0.5 - 5.5GHz$ CMOS distributed amplifier'. *IEEE Journal of Solid State Circuits*. 2000 February; **35**(2):231–239.

[19] CHOI K., ALLSTOT D.J.: 'Parasitic-aware design and optimization of a CMOS RF power amplifier'. *IEEE Transactions on Circuits and Systems I*. 2006 January; **53**(1):16–25.

[20] CHOI K., PARK J., ALLSTOT D.J.: 'Parasitic-aware Optimization of CMOS RF Circuits'. Kluwer Academic Publishers; 2003.

[21] CHU M., ALLSTOT D.J., HUARD J.M., WONG K.Y.: 'NSGA-based parasitic aware Optimization of a $5GHz$ Low-noise VCO'. In: Proceedings of the Asia South Pacific Design Automation Conference); 2004. p. 169–174.

[22] KOUGIANOS E., MOHANTY S.P.: 'Impact of Gate-Oxide Tunneling on Mixed-Signal Design and Simulation of a Nano-CMOS VCO'. *Elsevier Microelectronics Journal*. 2009 January; **40**(1):95–103.

[23] ZHANG G., DENGI A., CARLEY L.R.: 'Automatic Synthesis of a $2.1GHz$ SiGe low noise amplifier'. In: Proceedings of the IEEE RFIC Symposium; 2002. p. 125–128.

[24] BASU S., KOMMINENI B., VEMURI R.: 'Variation Aware Spline Center and Range Modeling for Analog Circuit Performance'. In: Proceedings of the International Symposium on Quality Electronic Design; 2008. p. 162–167.

[25] NOURANI M., RADHAKRISHNAN A.: 'Testing On-Die Process Variation in Nanometer VLSI'. *IEEE Design and Test of Computers*. 2006 June; **23**(6):438–451.

[26] GHAI D., MOHANTY S.P., KOUGIANOS E.: 'A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-VDD SoCs'. In: Proceedings of the International Symposium on Quality Electronic Design; 2008. p. 257–260.

[27] MOHANTY S.P., GHAI D., KOUGIANOS E.: 'A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-VTh Nano-CMOS VCO'. In: Proceedings of the 23rd IEEE International Conference on VLSI Design (ICVD); 2010. p. 99–104.

[28] BAKER R.J.: 'CMOS: Circuit Design, Layout and Simulation'. IEEE Press; 2003.

[29] HAGER W.W., ZHANG H.: 'Algorithm 851: CG-DESCENT, A Conjugate Gradient Method with Guaranteed Descent'. *ACM Transactions on Mathematical Software*. 2006 March; **32**(1):113–137.